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Digitally Modulated Bit Error Rate Measurement System for Microwave Component Evaluation

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Summary

The NASA Lewis Research Center has developed a unique capability for evaluation of the microwave components of a digital communication system. This digitally modulated bit-error-rate (BER) measurement system (DMBERMS) features a continuous data digital BER test set, a data processor, a serial minimum shift keying (SMSK) modem, noise generation, and computer automation. Application of the DMBERMS has provided useful information for the evaluation of existing microwave components and of design goals for future components. This paper describes the design and applications of this system for digitally modulated BER measurements.

Introduction

Since 1978, the Space Electronics Division of NASA Lewis Research Center (Lewis) has fostered the development of Ka-band satellite communications (30 GHz uplink, 20 GHz downlink) to ease the frequency and orbital congestion of U.S. commercial communications satellites at lower frequencies. In support of this goal, Lewis has conducted studies to assess communications demands and establish technical goals, funded development of proof-of-concept hardware models of critical components, initiated the development of the Advanced Communications Technology Satellite (ACTS) to demonstrate onboard switching and processing technologies, and established the Systems Integration, Test, and Evaluation (SITE) project to enable laboratory-based verification of advanced components and system architectures.

The SITE facility integrates many of the proof-of-concept models with custom hardware and software into a flexible simulation of a satellite-switched, time division multiple access (SS-TDMA) system at Ka-band frequencies. This facility is used to test and evaluate components, subsystems, and network architectures in a true system environment (ref. 1).

A unique feature of the first phase of the SITE project is its ability to measure the digital BER contribution of microwave components using a digitally modulated data source as a reference. In its second phase the SITE facility will enable bursted BER measurements and bursted data communications simulation. This paper describes the primary features, applications, and future direction of a digital communications system evaluation that uses the technique of measuring BER on continuously modulated data.

Digitally Modulated Bit-Error-Rate Measurement System

End-to-end BER is an important performance measure of the digital transmission characteristics of a communication system. Noise-susceptible analog and microwave components of the Earth station and satellite combine with transmission and propagation effects to degrade the quality of a digitally modulated signal. A measure of the amount of this degradation is the ratio of the number of bits received in error to the number of total bits received in a specified time, that is, the bit error rate (BER). The DMBERMS (fig. 1), developed for the SITE facility, provides an easy mechanism to measure BER performance of individual or cascaded components of a communication system, relative to a baseline standard.

Operational Overview

The hardware configuration of the DMBERMS is shown in figure 2. The DMBERMS consists of five subsystems and the microwave components being evaluated. Pseudorandom 64-bit digital data words at 3.456 million words per second are created in the data generator for a total throughput rate of nominally 220 megabits per second (Mbps). The data processor subsystem buffers the pseudorandom serial data, inserts a demodulator preamble, scrambles the data, and provides the data in a serial format to a serial minimum shift keying (SMSK) modulator. The modulated signal is then combined with a noise signal in the noise generation unit enabling variations in the signal-to-noise ratio to be applied to the components under test. The microwave output is converted back to a digital bit stream by an SMSK demodulator. The data processor then unscrambles, buffers, and transfers these data to the data checker in a 64-bit parallel format. The data checker compares the received data with the reference data and calculates the number of erroneous bits received. The BER is displayed on the data checker front control panel. Computer control of the data generator, data checker, and noise generation unit enables test automation.

The following sections describe the operation of each of the five main subsystems of the DMBERMS: data generator and data checker, modem and interference, noise generation, data processor, and computer control, followed by a description of the past and current DMBERMS applications.

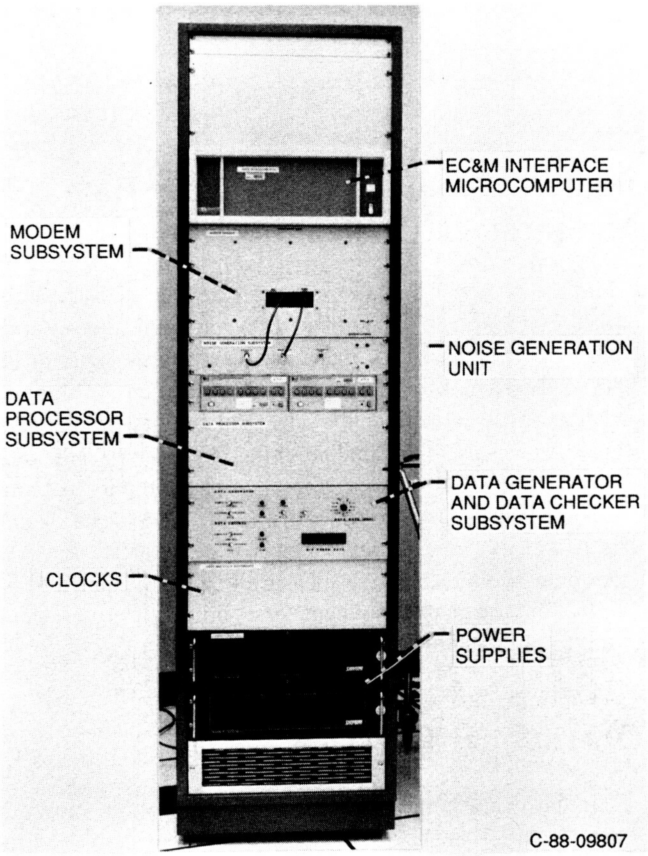


Figure 1.—Digitally modulated bit-error-rate measurement system.

Data Generator and Data Checker Subsystem

Bit-error-rate measurements are provided for the DMBERMS by a single chassis test set, called the data generator and checker, designed at NASA Lewis for the SITE project. Although housed in a single chassis, the data generator and checker were designed to be operationally independent by providing closed-loop reference data within the data checker for comparison with the received data. This feature enables any data checker to operate with any other data generator regardless of the physical distance or signal delay between them.

To implement this closed-loop reference method, the data generator creates a reproducible digital bit pattern and inserts a heavily error-encoded control word into a known location in the transmitted data stream. From the control word, the data checker can derive enough information about the original bit stream to recreate the data transmitted by the data generator. The error-free recreated data can then be compared with the received data to check for individual bit errors.

Data Generator

The DMBERMS data generator consists of two wire-wrapped circuit boards: a data generator board and a user interface board (fig. 3). The data generator board creates pseudorandom, continuous digital data at an information rate of 220 Mbps, output in 64-bit words to the data processor. Throughout this paper, the data created by the data generator will be referred to as the "source data sequence."

The source data sequence is created by a hard-wired, pseudorandom mapping of the outputs of two eight-bit up/down counters. This data creation method produces a bit pattern that repeats every 65 536 words. Control words are

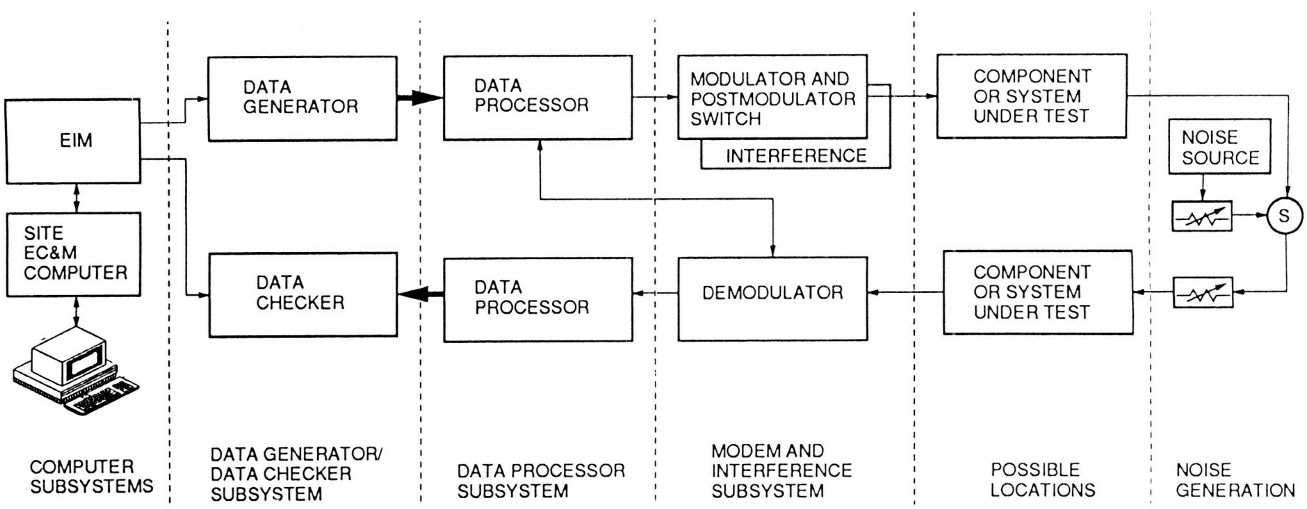


Figure 2.—Modulated data BER measurement system hardware configuration diagram.

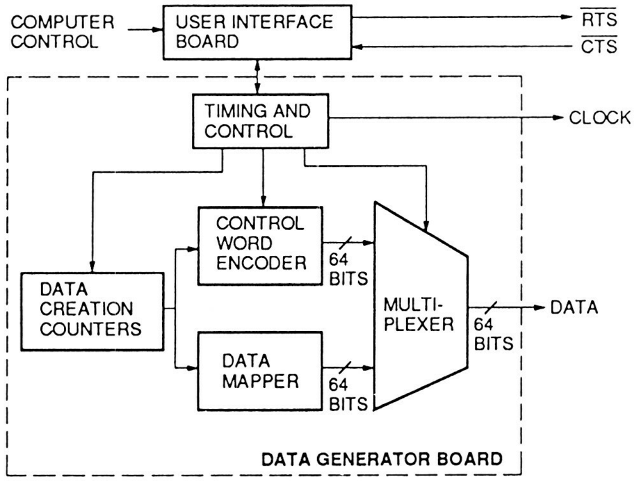


Figure 3.—Data generator.

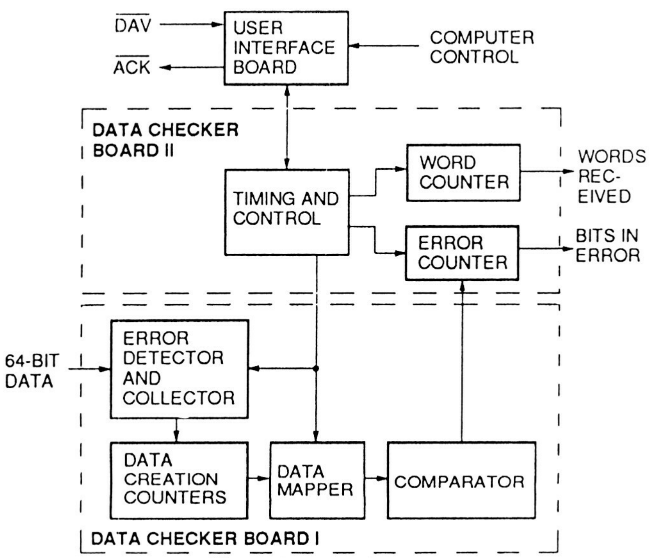


Figure 4.—Data checker.

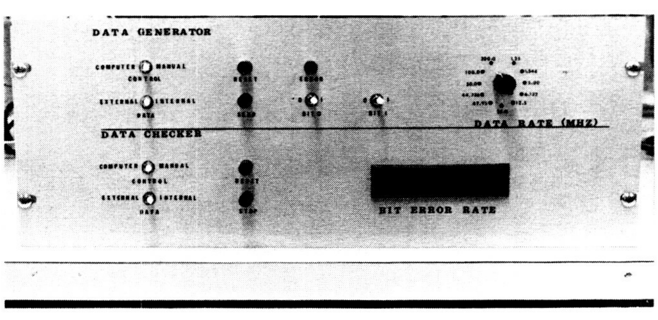


Figure 5.—Data generator and data checker.

created on the data generator board by error encoding the initial state of the data generation counters. A modified Hamming code is used to detect up to two errors out of every seven received bits and to correct one error out of every seven received bits. Beginning with the first transmitted word, control words are periodically multiplexed between data words.

Automated control of the data generator for initiation and termination of data transmission is provided through the user interface board. The user interface board also provides the control signals necessary to interface the data generator to the data processor chassis. When the data generator is ready to transmit data, the user interface board creates a request-to-send ($\overline{\text{RTS}}$) signal to the data processor. The data generator will begin transmitting when the data processor gives a clear-to-send ($\overline{\text{CTS}}$) signal to the data generator user interface board.

Data Checker

The DMBERMS data checker consists of three wire-wrap circuit boards: two data checker boards and a user interface board (fig. 4). The first data checker board receives the 64-bit parallel data (referred to hereinafter as the "received data sequence") from the data processor. A control word will be the first word received by data checker board I. Error checking and correction is performed on the control word, and its contents are used to initialize data regeneration counters that recreate the exact source data sequence. The recreated data sequence is then compared, bit-by-bit, with the received data sequence.

From the bit-by-bit comparison, data checker board II counts both the number of bits received in error and the number of total bits received, enabling the BER to be calculated. Data checker board II also contains all the timing and control circuitry for both data checker boards.

The user interface board performs the calculation of the BER in hardware and displays it on the front panel. As an alternative, the user interface can transfer the counts of bits in error and total received bits to a experiment control and monitor (EC&M) computer for BER calculation and data storage. The user interface also provides the necessary control signals to establish communication between the data checker and the data processor. When transmission is ready to begin, the data processor sends a data available ($\overline{\text{DAV}}$) signal to the data checker user interface board. The user interface board sends an acknowledge ($\overline{\text{ACK}}$) signal when it is ready to receive data.

A photograph of the data generator and checker chassis is shown in figure 5. A more comprehensive discussion of the data generator and data checker BER test set is contained in reference 2.

Modem Subsystem

The modem subsystem of the modulated data BER measurement system (DMBERMS) contains the modem (modulator-demodulator pair), logic level translators, a circuit to stretch the duration of the unique-word detection pulse from the demodulator, a postmodulator switch, and isolators (fig. 6).

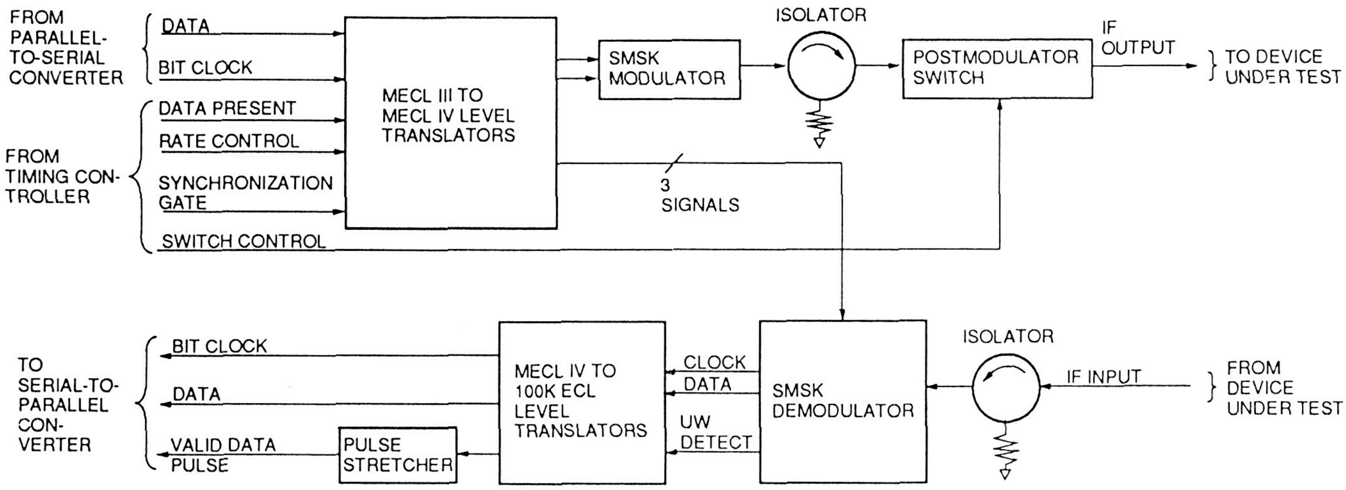


Figure 6.—Modem subsystem block diagram.

Serial Minimum Shift Keyed (SMSK) Modem

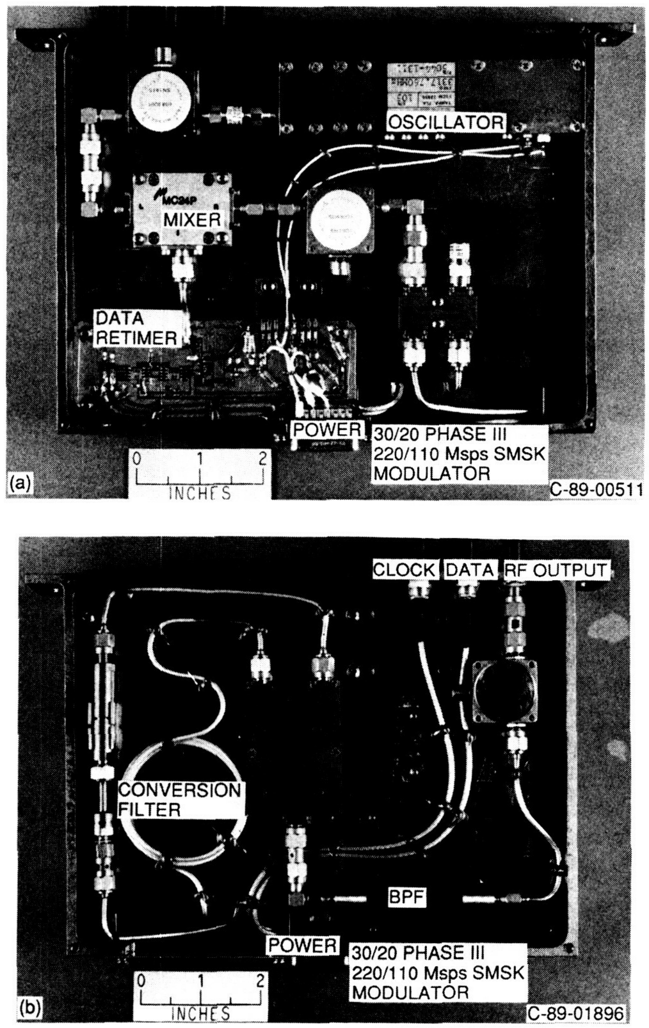
The SMSK modem for the DMBERMS was developed by the Government Electronics Group of Motorola, Inc., of Scottsdale, Arizona, under the third phase of the baseband processor proof-of-concept contract (NAS3-22502). Four sets of proof-of-concept modems were fabricated under the contract and delivered in November 1984. The DMBERMS uses SMSK primarily because it is the modulation scheme selected for Lewis' Advanced Communications Technology Satellite (scheduled for launch in the early 1990's) and because the effects of microwave components and link degradations on SMSK modulated signals were not well known.

The modem was designed to support two rates, a full rate of 221.184 megasymbols per second (Msps) and and a half rate of 110.592 Msps, and to provide rapid, independent burst acquisition (within 256 symbols or about 1.2 μsec in the full rate mode). In the half-rate mode (nominally 110 Msps) the demodulator was designed to produce a two-bit, soft-decision output (sign and magnitude bits) for use with an optional decoder. Only the full-rate mode (nominally 220 Msps) has been used in the DMBERMS application.

SMSK Modulator

Theoretically, minimum shift keyed modulation systems provide identical BER performance to the more traditional quadrature phase shift keying (QPSK) systems with a significantly higher concentration of signal energy near the center of the power spectrum (ref. 3). This improved spectral efficiency is especially important in bandwidth and power-limited satellite communications systems using nonlinear power amplifiers.

Serial minimum shift keying refers to the serial implementation of the MSK modulation scheme. The modulator (fig. 7) converts synchronized serial digital data and clock inputs into SMSK modulated data. As shown in the modulator block diagram (fig. 8), the SMSK waveform is created from a binary phase modulated signal by a bandpass conversion filter whose center



(a) Top view.
(b) Bottom view.

Figure 7.—220-Msps SMSK modulator.

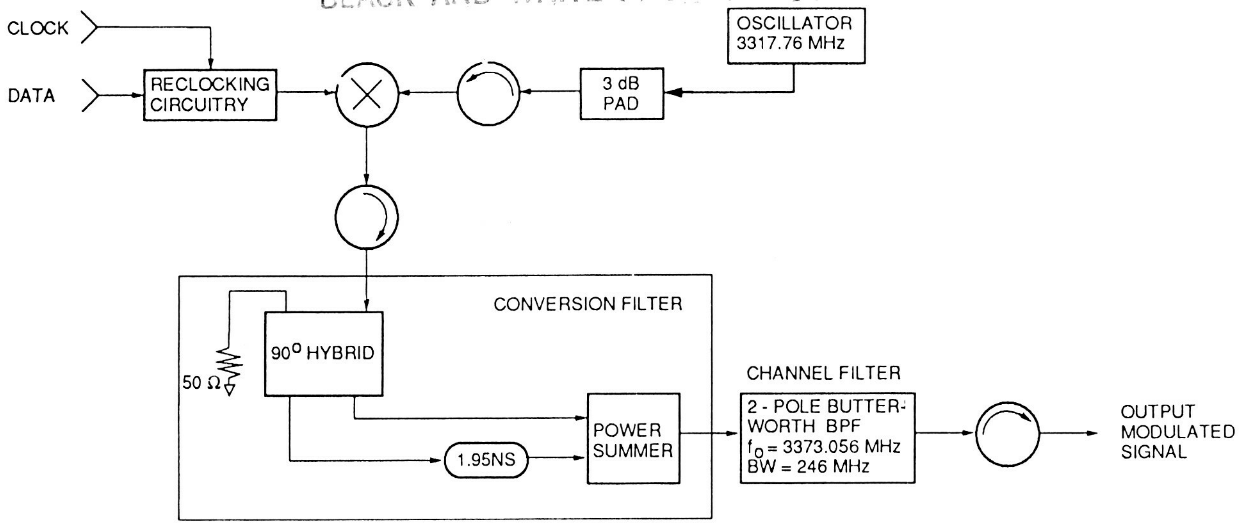


Figure 8.—220-Msps SMSK modulator block diagram.

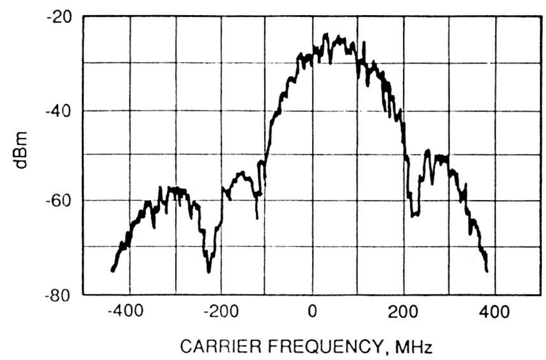


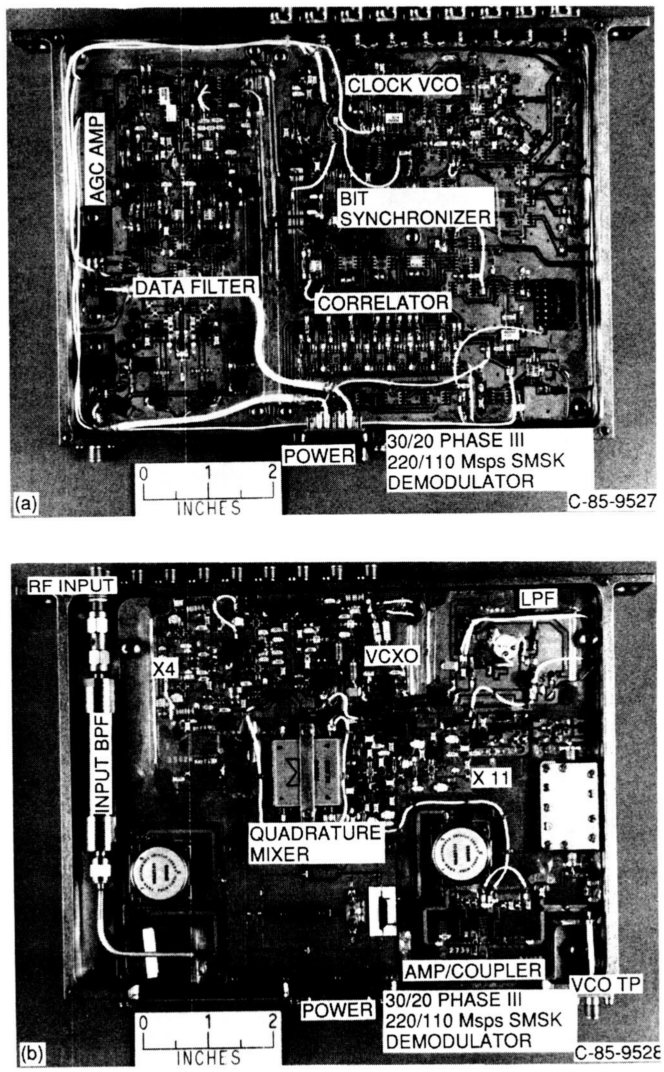
Figure 9.—220-Msps SMSK modulator power spectrum.

frequency is one quarter of the data rate ($R/4$ or 55.296 MHz for the full-rate mode) higher than the carrier frequency (3317.76 MHz). The SMSK output spectrum has a null-to-null main lobe bandwidth of one and one-half times the data rate ($3R/2$ or 332 MHz nominally), a center frequency of 3373.056 MHz, and a symbol rate equal to the baseband digital data rate (221.184 Msps). The SMSK spectrum for 220 Msps operation is shown in figure 9.

To check the integrity of remote microwave links and aid the alignment of receiving equipment, the modulator can produce an apparently unmodulated carrier. This is accomplished by selecting a baseband data sequence of all logic ones as the modulator input via a modem chassis front panel switch. The SMSK modulated spectrum is then simply the carrier frequency of 3317.76 MHz.

Serial Minimum Shift Keying Demodulator

The demodulator (fig. 10) converts an SMSK modulated carrier into synchronized serial digital data and clock outputs. As shown in the demodulator block diagram (fig. 11), the input signal is bandpass filtered to reduce the effects of adja-



(a) Top view.
(b) Bottom view.

Figure 10.—220/110-Msps SMSK demodulator.

cent channel interference. The demodulator consists of a carrier tracking loop, bit synchronization and timing control loops, and unique-word detection circuitry.

The demodulator was designed to operate in a burst mode, and can accommodate up to a 60-kHz deviation in carrier frequency and a 20-dBm variation in input power from burst to burst. Much of the demodulator circuitry was designed to enable rapid, independent burst acquisition and dual rate operation. In the DMBERMS the demodulator acquires timing at the start of each burst corresponding to a new test condition. The burst consists of a modulated preamble followed by a continuous, uninterrupted modulated data sequence. The required burst duration may range from milliseconds to several minutes depending on the expected BER for each test condition.

Modem Performance

Acceptance testing of the modem was performed by Motorola under seven input power and burst duty cycle combinations. Several of the acceptance test conditions were duplicated by NASA Lewis personnel. A noise generation unit was fabricated to provide the discrete signal-to-noise ratios required to evaluate back-to-back modem performance.

The demodulator can accept input power levels from −28 to −48 dBm and burst duty cycles as low as 1 percent. The test condition used to establish the baseline BER performance of the DMBERMS operating environment is an input power of −33 dBm and 100 percent burst duty cycle (continuous signal following initial burst acquisition). The plot of BER versus E_b/N_o (where E_b is the energy per bit and N_o is the noise power density) for this condition, as measured by both Motorola and NASA Lewis, is shown in figure 12(a). Small discrepancies at low E_b/N_o result from Motorola's method of counting adjacent bits in error as a single bit error. Plots of BER versus E_b/N_o for three of the seven input power and burst duty cycle combinations are shown in figure 12(b). Virtually no performance degradation has been observed in the modem operation over more than 4 years of operation.

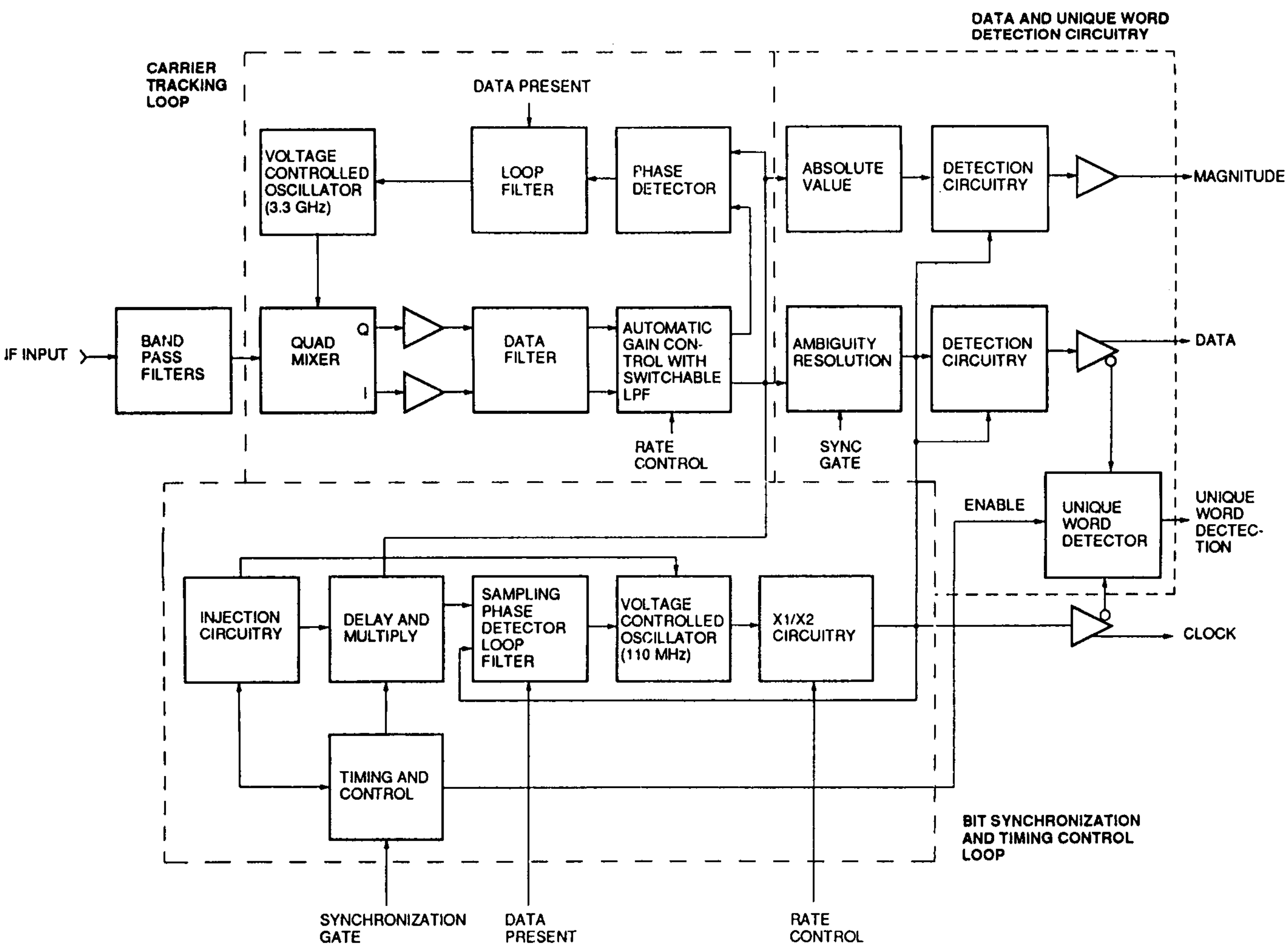


Figure 11.—220/110-Msps SMSK demodulator block diagram.

Modem Control Signals

Although the DMBERMS uses the modem in a continuous data mode (that is, a single burst per test condition), several demodulator control signals along with an acquisition preamble are required for proper operation. All control signals and the preamble are created by the data and timing controller board of the data processor subsystem. Selection of the 220 or 110 Msps rate of operation is accomplished via the rate control input. Rate control changes the data filter bandwidth and clock (voltage controlled oscillator) frequency. A logic low selects full rate, 220-Msps operation; a logic high selects half rate, 110 Msps.

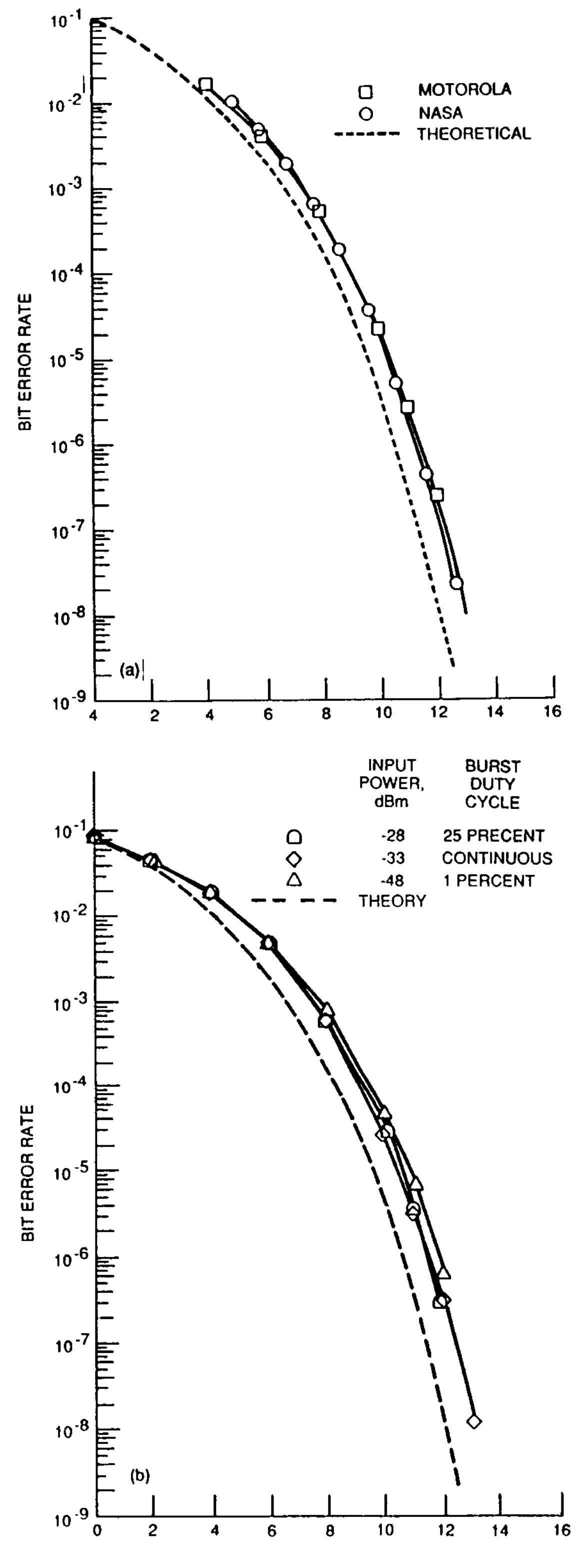
Two coarse timing signals (data present and synchronization gate) assist the demodulator acquisition and tracking loops in locking onto the incoming modulated carrier, deriving a synchronous symbol clock, and resolving phase ambiguities. The data present signal is activated only during the expected duration of the burst to prevent charge buildup on the carrier and clock phase-locked-loop capacitors when no data are present. The synchronization gate signal is used to resolve data phase ambiguity introduced by the carrier loop. The timing of data present and synchronization gate signals is adjusted by the data processor to accommodate a variety of signal propagation delays through microwave components and links under test.

The demodulator acquisition preamble consists of a specific 256-bit sequence (ending in a 7-bit unique word) that enables the demodulator to completely recover the incoming data and produce a real-time unique-word-detection pulse to indicate the start of valid demodulated data.

Even though the DMBERMS makes BER measurements on continuous data, the modem operates in a burst mode with one long burst for each BER measurement. The burst arrival-time tolerance designed into the demodulator allows bursts from independent users to vary by as much as ±60 nsec from the demodulator control signal timing. In the DMBERMS this tolerance is used to accommodate most of the fine timing uncertainty created by different signal propagation delays through various microwave components and links under test. As long as the signal propagation delay is within the 120-nsec window, no adjustment of the control signal timing is necessary. The data and timing controller board of the data processor subsystem can adjust the modem control signal timing to accommodate additional microwave path delays of up to 192 nsec in 6-nsec increments in addition to coarse, bulk delays.

Level Translators/Pulse Stretcher

All digital signals to and from the modem are at Motorola emitter coupled logic (MECLIV) levels. Zero volt represents a logic high, and −0.5 V represents logic low. In order to be compatible with commercial MECL III and 100K series ECL logic, level translators were designed and fabricated for the modem control signals (rate control, synchronous gate,



(a) Baseline BER curve.
(b) Family of BER curves.

Figure 12.—Bit error rate performance curves for Motorola SMSK modem.

and data present), baseband data and clock input and output, and demodulator unique-word detect output.

The parallel-to-serial converter of the data processor subsystem provides the serial baseband data stream and synchronized clock inputs to the MECL III-to-IV level translator that precedes the modulator. The demodulator data, clock, and unique-word-detection pulse outputs are sent to the MECL IV-to-100K series ECL level translator (fig. 6).

After translation to 100K series ECL logic levels, the duration of the unique-word-detection pulse is stretched from 4.5 nsec (1 bit duration) to 20 nsec as required by the custom serial-to-parallel converter. The demodulated data, the resynchronized clock, and the stretched unique-word-detection pulse are then passed to the serial-to-parallel converter of the data processor subsystem at 100K series levels for conversion to 64-bit words.

Postmodulator Switch

The modem subsystem was designed for application in both the continuous DMBERMS and the bursted TDMA ground terminals of future SITE project phases. Bursts of modulated data are created by a PIN diode switch immediately following the SMSK modulator. This postmodulator switch is used to create one very long burst of modulated data for the duration of each continuous BER measurement.

More importantly, the postmodulator switch was used to verify proper demodulator acquisition (as indicated by unique-word-detection and zero BER under noiseless input conditions) on the first and every successive acquisition attempt over the full range of input carrier frequencies (3317.76 MHz ±30 kHz), input power (−33 to −55 dBm), and input burst arrival times (0 ± 60 nsec).

The postmodulator switch is an EMCO model 18203-SW-E 71 PIN diode switch with a 1.0- to 4.0-GHz operational bandwidth and TTL digital control of switch closure. Lewis in-house characterization of switch performance showed greater than 60-dB isolation in the open (burst off) state, less than 1.0-dB insertion loss in the closed (burst on) state, and less than a 40-nsec turn-on and turn-off delay from TTL control level transitions to the 95-percent amplitude points.

While a voltage standing wave ratio (VSWR) was measured to be less than 1.5 with the switch closed, a VSWR of up to 25 was measured in the open state. Consequently, isolators were used on either side of the postmodulator switch to prevent the possibility of damage to adjacent microwave components (especially the modulator) due to excessive reflected power.

Interference Modem Subsystem

A second, nearly identical, modem subsystem was fabricated to enable an examination of adjacent and cochannel interference effects on BER in a multichannel transponder simulation. To ensure the integrity of the BER measurements on the desired channel, power supplies and local oscillators for the two chassis were physically separate from and independent of each other.

A 100K series ECL shift register implementation of a $2^{16} - 1$ bit pseudonoise sequence generator was used as the source of digital data for the interfering modulator. Since recovery of the pseudonoise sequence was not required, the pseudonoise sequence generator ran completely asynchronously with respect to the data generator for the desired channel. The center frequency and amplitude of the interfering channel was set by the test operator using a frequency converter and attenuator external to the interference chassis.

Noise Generation Unit

In a digital system the signal-to-noise ratio represented by E_b/N_o, is a measure of the relative levels of the available signal power and noise power input to a component under evaluation. The E_b/N_o affects the component's ability to carry digital information (ref. 4). In general, a low E_b/N_o increases errors in the transmitted digital information, while a higher E_b/N_o results in fewer errors. The BER is a measure of the relative number of errors in the data. Measured BER at specific E_b/N_o values is used to characterize the performance of the component being evaluated over a wide range of operating conditions (fig. 12(b)). For each curve in the figure, the total input power (signal and noise combined) is fixed, and the E_b/N_o is varied, resulting in a range of BER values.

In the DMBERMS the E_b/N_o is varied by the noise generation unit (fig. 13). The power level of the noise signal, simulated by a solid-state white noise source, is regulated with a step attenuator. The digitally modulated carrier is added to the attenuated noise signal with a microstrip combiner. A se-

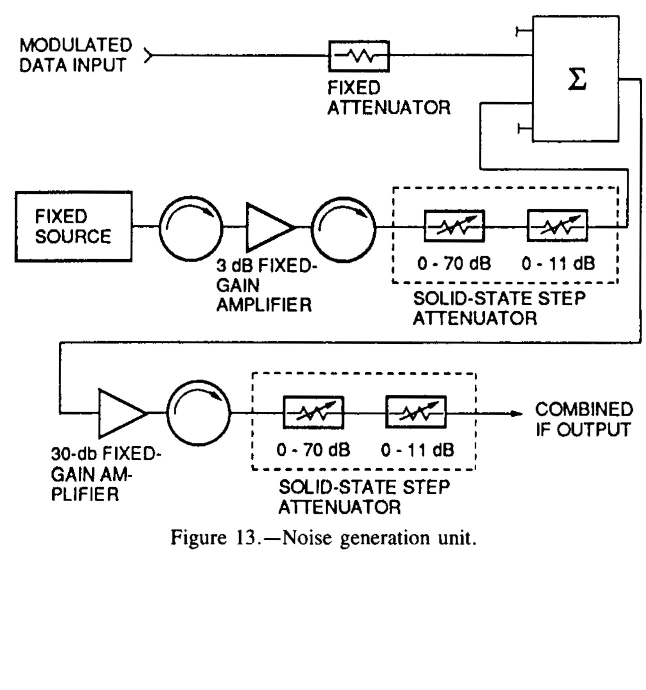


Figure 13.—Noise generation unit.

cond step attenuator is used to control the power level of the combined signal and noise. Both step attenuators can be adjusted to allow either the E_b/N_o to be varied while the total power level is held constant or the total power to be varied while the E_b/N_o is held constant. The baseline performance of the DMBERMS was established by connecting the SMSK modulator and demodulator back-to-back through the noise generation unit and measuring BER for each E_b/N_o setting. The combined power level into the demodulator was fixed at −33 dBm. For accurate comparison of the baseline curve with any BER curves for a component under evaluation, the input power to the demodulator must be adjusted to exactly −33 dBm.

The component under evaluation can be inserted into the DMBERMS in either of two places: between the modulator and the noise generation unit, or between the noise generation unit and the demodulator (fig. 2). The choice of location depends on the type of test and the characteristics of the component itself. In the first location the BER performance of the component under noise-free input signal conditions can be measured. In the second location the BER performance of the component can be measured under varying input power and E_b/N_o conditions.

The actual E_b/N_o value is determined from noise power P_n and signal power P_s measurements according to the following equation (ref. 5):

$$E_b/N_o = (P_s/P_n)(N_{bw}/R)$$

where N_{bw}, the noise bandwidth of calibration filter, is equal to 379.69 MHz and R, the data rate is equal to 221.184 MHz. Therefore, in the DMBERMS

$$E_b/N_o = 1.7166(P_s/P_n)$$

A more comprehensive discussion of the noise generation unit may be found in references 6 and 7.

Data Processor Subsystem

The data processor subsystem of the DMBERMS performs functions similar to a TDMA (time division multiple access) controller of a satellite-switched TDMA Earth station. The data processor (fig. 14) consists of five TTL and ECL logic boards: a data and timing controller board, transmit and receive FIFO (first-in, first-out) memory/scrambler boards, and the parallel-to-serial and serial-to-parallel converter boards.

The data and timing controller board formats and routes digital user data, generates the modem control signals, and maintains system timing. The transmit and receive FIFO memory/scrambler boards buffer, scramble, and descramble baseband data flow between the data generator and checker subsystem and the modem subsystem. The parallel-to-serial and serial-to-parallel converters create the serial data interface to the modem subsystem.

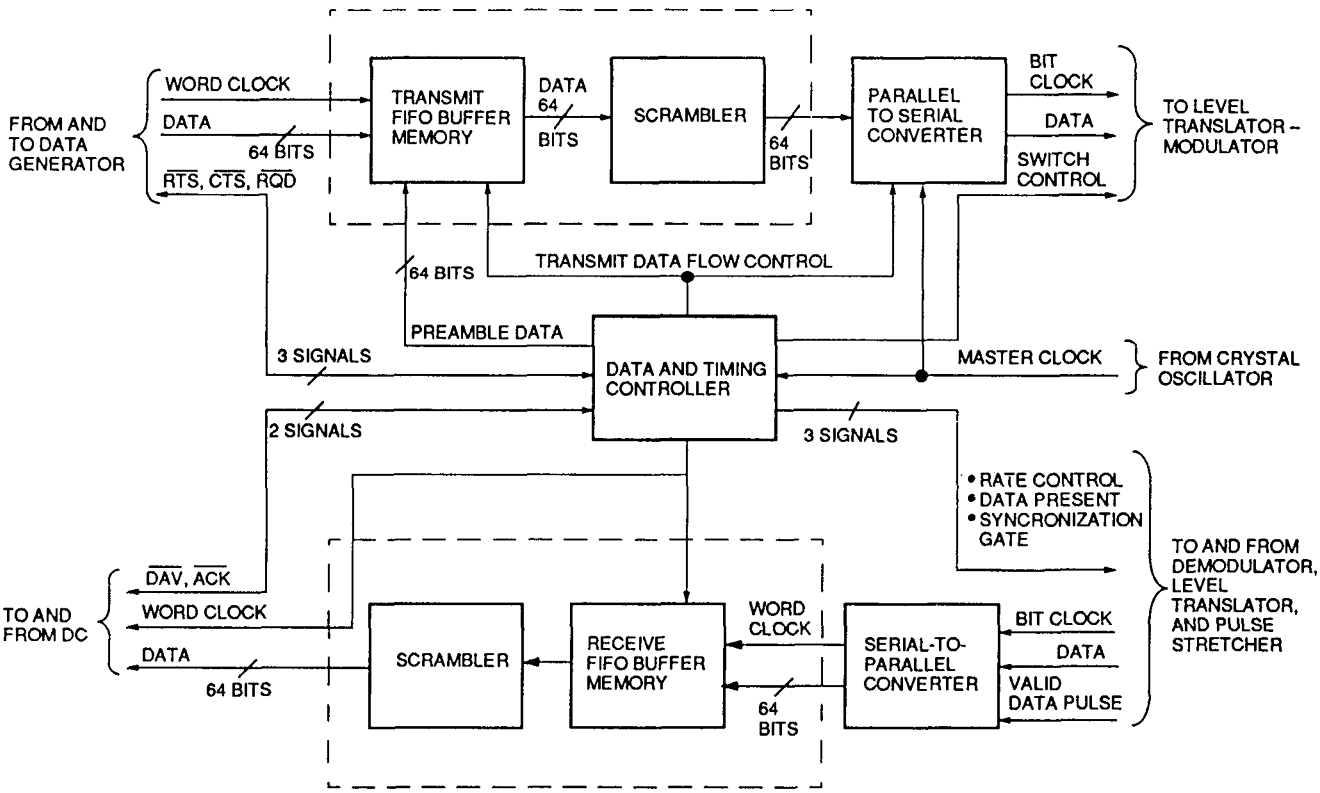


Figure 14.—Data processor subsystem block diagram.

One major difference between the function of the DMBERMS data processor and an Earth station TDMA controller is the absence of periodic bursting of data at a higher speed than the user data throughput rate. In the DMBERMS the data processor operates on user (data generator) data as if they were one long, continuous burst instead of many shorter bursts and as if the user data rate and modem burst rate were equal.

The function of each board in the data processor subsystem will be described somewhat independently. The data and timing controller board description will address the interaction of the various board and chassis functions to create a continuous data BER measurement system.

Transmit and Receive FIFO Memory/Scrambler Boards

Parallel data flow between the data generator and checker subsystem and the data processor subsystem through nearly identical transmit and receive FIFO memory/scrambler boards. These boards use first-in, first-out (FIFO) buffer memories to absorb timing differences among voltage controlled oscillators of the data generator and checker, the data processor, and the modem subsystems.

The 64-bit wide by 16-word deep FIFO memory in the transmit board is also used to insert the 256-bit demodulator preamble in front of the data generator's source data sequence. Once the preamble is stored in the FIFO memory, a periodic sequence of writes and reads appends the source data sequence to the preamble in synchronism.

In the receive board the FIFO memory absorbs clock frequency variation and timing distortions (within demodulator tolerances) caused by the propagation of the modulated signal through the microwave components and/or link under evaluation. In both transmit and receive boards, data read out of the FIFO memories is then scrambled. The purpose and method of scrambling are described below.

In the DMBERMS the data generator simulates the operation of a real communications system user by creating a variety of serial data patterns. User data created from real-world voice, video, or computer communications can contain long periods where no logic level transitions are present. To ensure that the SMSK demodulator maintains synchronization with the incoming data for the duration of the longest burst, a nearly uniform density of logic level transitions within the modulated data is required. Here, "density" refers to the number of logic level transitions (high to low and low to high) that occur over a number of bits of data.

Demodulator synchronization problems can arise when the incoming data are fixed at or biased to one logic level. Either condition can result in a long string of data fixed at one logic level and the increased probability of synchronization-induced errors. Motorola empirically determined an overall transition density of 0.45 to 0.55 over 64 bits of data as sufficient to maintain demodulator synchronization under all tested conditions.

To achieve this transition density, a pseudorandom sequence is used to scramble the incoming data, thereby limiting the duration of output data at one fixed logic level. The transmit FIFO memory/scrambler board uses a 63-plus 1-bit pseudorandom pattern to limit constant logic level strings to 6 bits when the incoming data are fixed at or biased to one logic level. The same pattern also significantly reduces the probability of constant logic level strings longer than 6 bits when the incoming data are more of a random nature.

This type of scrambling is not used for data encryption or security purposes, and it is not intended to meet CCITT or AT&T specifications for terrestrial telecommunications. It was chosen because of its ease of implementation and because it was sufficient to allow the demodulator to maintain synchronization during transmission of long BER measurement data sequences.

Scrambling is accomplished by the exclusive or (XOR) of each bit of the incoming BER measurement data sequence with the corresponding bit of the pseudorandom pattern. The scrambling function is implemented in parallel using 64 XOR gates. The scrambler board was designed to allow an external computer to download different 64-bit pseudorandom patterns onto the board or select a fixed scrambling pattern using onboard logic level switches.

Parallel-to-Serial—Serial-to-Parallel Converter Boards

The data flow between the data generator and checker and the data processor subsystems over 64-bit wide parallel interfaces at 3.456 million words per second. Parallel-to-serial and serial-to-parallel converter boards are used to transform these parallel data into serial data between the data processor and modem subsystems at 221.184 Mbps.

The method of controlling the timing of data flow between the converters and the modem differs from the transmit side to the receive side of the DMBERMS. On the transmit side the data and timing controller board coordinates data flow from the transmit FIFO memory/scrambler through the parallel-to-serial converter and on to the modulator. On the receive side of the DMBERMS, the demodulator data and synchronous clock outputs are precisely aligned with the demodulator unique-word-detection pulse. The demodulator clock and unique-word-detection pulse are used by the serial-to-parallel converter to write parallel data into the receive FIFO memory/scrambler. From this point the data and timing controller board again takes control of the data flow in synchronism with the data processor master clock. Careful coordination of data flow control between the data processor and modem subsystems ensures proper bit alignment at the data checker and valid BER measurement.

The parallel-to-serial and serial-to-parallel boards were fabricated by Multiwire Corp. using board layouts and wire lists developed at NASA Lewis. The Multiwire Corp. fabrication technique was selected over the Lewis wire-wrap technique because of the boards' very high speed of operation, the proximity of the advanced Schottky TTL and ECL chips on the board, and the difficulty of distributing the multiple power and ground supplies required by both logic families. The ECL level serial inputs and outputs are driven differentially between the

converter boards and the level translators of the modem subsystem.

Data/Timing Controller Board

The data and timing controller board exercises the data communication protocol with the data generator and checker subb system, controls the operation of the other boards in the data processor, creates the control signals for the modem, and controls the flow of data among the three subsystems.

To start transmission of BER measurement data through the DMBERMS, the data and timing controller first exercises a simple connection protocol with both the data generator and the data checker. When the data generator is ready to begin producing test data in the form of 64-bit parallel words, it generates a request-to-send ($\overline{\text{RTS}}$) signal. The data and timing controller then notifies the data checker that received data are imminent by generating a data available ($\overline{\text{DAV}}$) signal. The data checker may respond with an acknowledgment ($\overline{\text{ACK}}$) that it is ready to receive data. If the communications path has not yet been established or if the data checker is not ready for any other reason, the data and timing controller returns a request denied ($\overline{\text{RQD}}$) signal to the data generator and waits for another request. Else, the data/timing controller initializes itself and the rest of the data processor and modem subsystems for the start of a test.

During initialization, the data and timing controller resets its bit and word counters, returns the modem control signals to their off-state, and resets all other boards in the subsystem. It then downloads a prescrambled version of the 256-bit demodulator preamble memory from onboard read-only memory (ROM) into the transmit, FIFO buffer memory. The XOR function of the scrambler restores the preamble data to the proper pattern when the user data begin to flow through the FIFO memory/scrambler board.

Once initialized, the data and timing controller board returns a clear-to-send ($\overline{\text{CTS}}$) to the data generator signifying that the communications link has been established and test data generation can begin. When the data generator receives the $\overline{\text{CTS}}$, it begins sending 64-bit words of the source data sequence to the transmit FIFO memory/scrambler board. Source data words are thus appended to the preamble data words already stored in the FIFO memory.

Each word read out of the transmit FIFO memory is scrambled by the bank of XOR's and appears at the input latch of the parallel-to-serial converter after a short propagation delay. The data and timing controller board simultaneously strobes each word into the parallel-to-serial converter and reads the next word out of the transmit FIFO memory/scrambler board.

After the first source data word is strobed into the parallel-to-serial converter, the data and timing controller sends a start pulse to the parallel-to-serial to begin serial data output. Once started, only periodic strobes are required to keep the parallel-to-serial converter running. Each successive write of source data words into the transmit FIFO memory/scrambler causes a strobe of the scrambled data output word into the parallel-to-serial converter and another read from the FIFO memory.

To this point, the transmit portion of the data processor subsystem has appended the scrambled source data sequence to the 256 bits of the now proper preamble unique-word sequence. About 50 nsec before this serial stream reaches the modulator, the data and timing controller opens the post-modulator switch and SMSK modulated data soon appear at the modulator output. This modulated signal is mixed with noise from the noise generation unit, attenuated, and passed through the microwave components or link under evaluation.

Depending on the components or link being evaluated, the modulated signal that returns to the demodulator has been delayed, degraded by noise from several sources, attenuated, and possibly shifted in frequency. Each of these degradations affect the demodulator's ability to recreate an error free digital data stream.

The received data sequence and clock recovered by the demodulator is processed by the receive side of the data processor subsystem in the inverse order of the transmit side operations. The preamble unique-word sequence is stripped from the data sequence by ignoring the demodulator output until receipt of the unique-word-detection pulse. The synchronized serial data and clock streams are translated to ECL logic levels and then converted into 64-bit parallel words by the serial-to-parallel converter. One by one, these words are clocked into the receive FIFO memory/scrambler board in synchronism with the demodulator recovered clock.

Any burst arrival time variation (within the demodulator's ± 60-nsec tolerance) and symbol frequency variation (produced by the components under evaluation) will propagate through the serial-to-parallel converter and into the word clock used to write data into the receive FIFO memory/scrambler. In the DMBERMS the receive FIFO memory is used as an elastic buffer to absorb the timing differences between the recovered clock and the data processor master clock. The master clock used in the DMBERMS is a Vectron model CO-223 oven-controlled crystal oscillator with external voltage control and 5×10^{-11} short-term stability.

To ensure independence from recovered clock timing and proper FIFO memory operation, several words of recovered, scrambled data are written into the receive FIFO memory/scrambler before the data and timing controller enables the periodic reading of data out of the FIFO memory. The recovered data words are then read out of the receive FIFO memory in synchronism with the master clock, descrambled, and strobed into the data checker's input latch. Each successive FIFO memory read causes a simultaneous write into the data checker. From there, the data checker processes the received data sequence and computes BER as described previously.

The process of transmitting and receiving the data sequence through the microwave components or link under evaluation continues uninterrupted until the test operator or controlling computer determines that a sufficient number of recovered bits have been received to perform a statistically valid BER calculation.

Test Automation

A controlling computer, called the experiment, control, and monitor (EC&M) computer, is used to make measurements and run experiments in the SITE facility, including the DMBERMS. The EC&M computer can adjust and read signal power levels at various test points in the SITE system hardware. It can also check the operational status of the system by monitoring appropriate signal lines and by receiving status information from various subsystems. A test engineer can enter the types of experiments to perform, the points to monitor, and parameters to control. Status information and data that the EC&M computer accumulates can be stored for later processing, and can be processed in real time for immediate display.

A large minicomputer, a Concurrent Computer Corporation (CCUR) model 3240, is used to perform the EC&M function. Because of the large size and difficulty in transporting the CCUR 3240 and because of the controlled environment that the computer requires, the EC&M computer is usually located remotely from the experiment. Remote control and monitoring via standard interfaces (RS-232, IEEE-488) avoids long cables with many parallel signal lines. Fiber optic interface extenders are used if the communication distance exceeds that of reliable RS-232 or IEEE-488 links.

Most of the microwave components and test instruments (primarily signal generators, attenuators, and power meters) within the SITE system are controlled by the EC&M computer using IEEE-488 interfaces. The EC&M computer control of the data generator and checker requires many parallel signal lines that can not be driven long distances. Therefore, control of the data generator and checker and of BER data acquisition is performed locally by a Motorola 6809-based microcomputer, called the EC&M interface microcomputer (EIM). Communication between the EC&M computer and the EIM is performed using a special command protocol over an RS-232 serial interface.

The EIM software, written in 6809 assembly language, creates appropriate control signals to the data generator and checker and sends status and raw BER data back to the EC&M computer as required. Control signals are created by the EIM through Intel SBC 519 programmable, input-output expansion boards. The EIM central processing unit (CPU) board controls the SBC 519 boards through a Multibus interface. A block diagram of the EIM hardware configuration is shown in figure 15.

The format of the messages between the EC&M computer and the EIM was designed to be easily readable and to allow command simulation by a terminal. All messages between the EC&M computer and the EIM consist of either two or three parts. The first part is the command destination. The second part is the function to be performed. If present, the third part is information. All messages are terminated with a carriage return. A sample of the command message format is DG1 START 1 2 0002. Here, DG1 indicates a message destination at generator 1. The command START initializes the DG1 and creates a transmission request to the ground terminal. The information following the START command specifies the data rate, the data type, and the destination checker.

If a message sent from the EC&M computer to the EIM is received error-free and is valid, the message is decoded and appropriate control signals are given to the data generator or data checker. The EIM sends a response (an $\overline{\mathrm{ACK}}$ signal, a STATUS message, or BER data) to the EC&M computer to acknowledge receipt of the command message. The NAK message (negative acknowledgement) is sent the EC&M computer if an invalid or an erroneous message is received. Table I shows the format of all the valid messages from the EC&M computer to the EIM and their acknowledgements. A flow chart of the EIM software is shown in figure 16. Reference 8 contains a more detailed discussion of the EIM.

The DMBERMS uses the EC&M computer to control the data generator, the data checker, and the noise generation unit, and to calculate and display the bit error rate. The EC&M computer can be configured by a test engineer to vary and read power levels on the component under evaluation and to control various laboratory instruments.

The EC&M function on the CCUR 3240 computer is performed in three phases: test definition, test execution, and posttest data presentation. During test definition, the test engineer interactively enters a test sequence and device list of instruments to be controlled or monitored (ref. 9). During test execution, the EC&M computer sets the signal-to-noise ratio in the noise generation unit, controls signal generators and attenuators, sets power levels, reads power meters, controls the data generator and checker, and reads BER data as required by the information from test definition phase. While the test is running, the EC&M computer periodically displays on a terminal the status

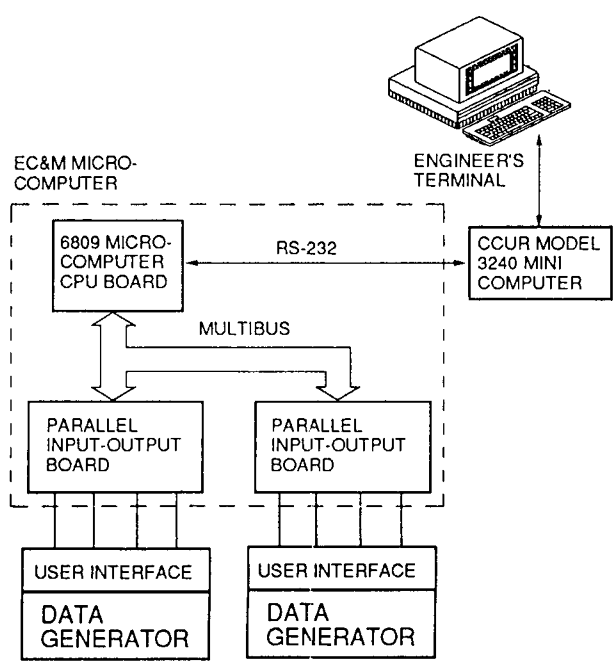


Figure 15.—EIM hardware configuration.

TABLE II.—MESSAGE FORMAT[a]

[Each character on chart represents one ASCII character.]

	Message	Acknowledgement
Data generator	DGx STOP User number	ACK
	DGx START r y dddd Destination Data type Rate User number	ECM DGx STATUS uuuuuuu t Transmission status: 1=started 2=denied 4=time out Unused User number
	DGx ERROR ee Bit in error User number	ACK
	DGx STATUS User number	ECM DGx STATUS uuu s dddd Destination Status: 0=inactive 1=active Unused User number
Data checker	DCx STOP User number	ACK
	DCx STATUS User number	ECM DCx STATUS uuu s uuuu Status: 0=inactive 1=active Unused User number
	DCx BER User number	ECM DCx BER uu wwwwwwwwww eeeeeeee Bit in error Words received Unused User number

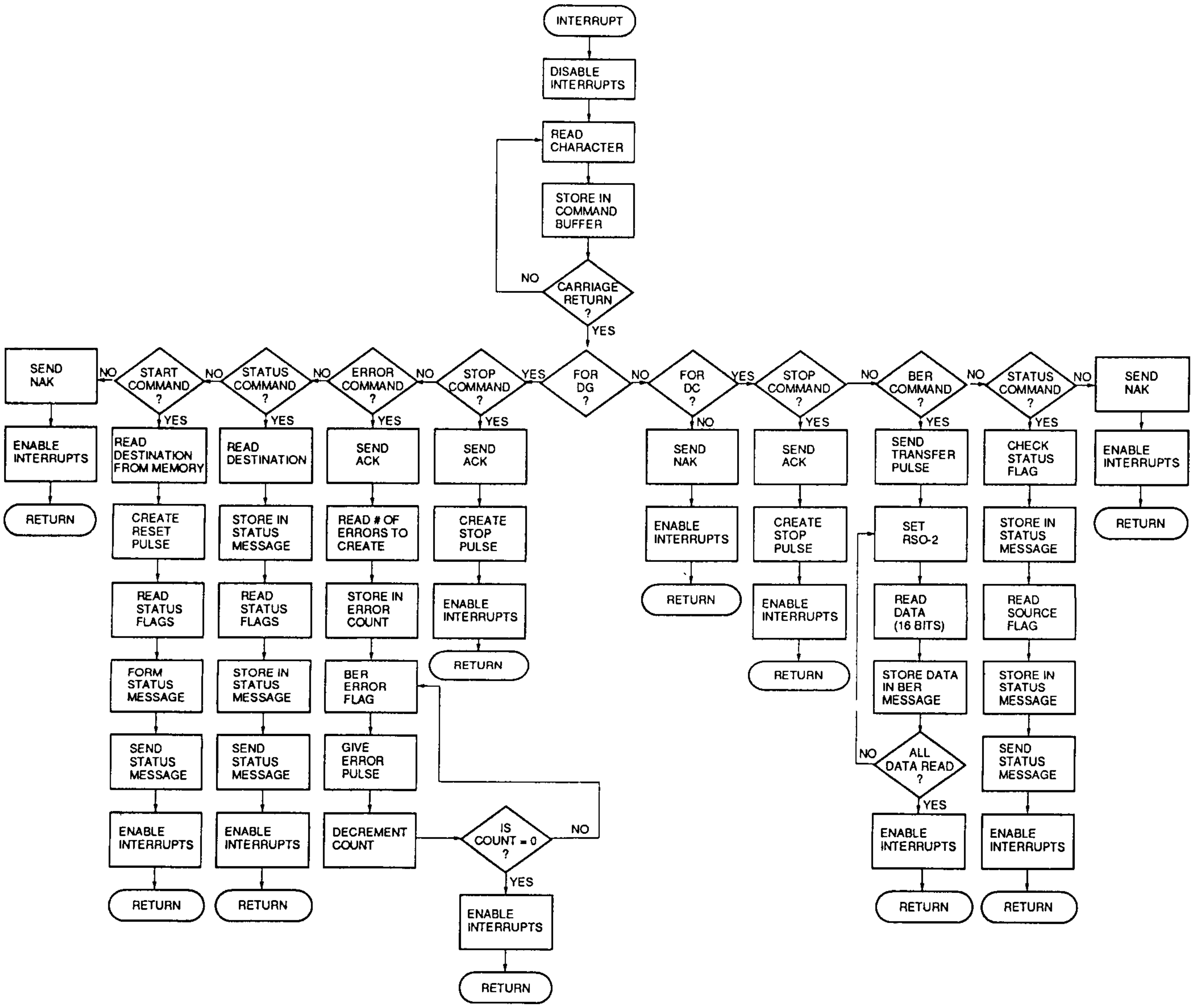


Figure 16.—EC&M microcomputer flow chart.

of the test and the latest data the computer has acquired. During the posttest data presentation phase, the EC&M computer either immediately prints the data it has acquired or processes it to obtain a particular printing format or graph.

For some short-term testing at remote locations, it is impractical and time consuming to construct a long-distance (out of building, for example) serial interface to the EC&M computer because of the short duration of the testing. In this case a small Sage Model IV 68000 microprocessor-based microcomputer replaces the EC&M computer. The Sage computer is portable and can be collocated with the DMBERMS at the test site. For simplicity, the Sage computer uses the EIM for control and data acquisition of the data generator and checker, just as the EC&M computer would. The Sage computer performs a subset of the EC&M functions: the control, monitoring, and data acquisition from the data generator and checker. All the other EC&M functions must be performed manually.

Test Operation

A typical test configuration consists of three major parts: the EC&M computer, the DMBERMS, and a component or link under evaluation. The EC&M computer runs a menu-driven program that allows a test engineer to configure the test environment including the tests to be performed and the instruments to be controlled and monitored. The test engineer can specify a time interval between BER measurements and a number of BER measurements to make for each test setting. Once the desired test configuration has been entered, the engineer executes the EC&M program to run the tests.

During the test execution phase, the EC&M computer first initializes the test instruments under its control and then sets the signal-to-noise ratio for the first test point. The EC&M then sends a START message to the EIM, which decodes it and resets the data generator. Next, the data generator activates the

request-to-send ($\overline{\text{RTS}}$) signal to the data processor, starting a connection protocol (described in the section "Data and Timing Controller Board") to establish a communication path to the data checker. When the data processor issues a clear-to-send signal, the data path has been established, and the data generator begins. The source data propagate sequentially through the components from the data generator and into the data checker as shown in figure 2 (p. 2).

The EC&M computer automatically acquires raw BER data from the data checker via a BER request command to the EIM. The EIM reads the BER data (number of bits in error and number of total bits received) from the checker through its user interface board. Then the EIM sends the BER data to the EC&M for BER calculation and storage.

After each BER measurement, the EC&M stops the BER measurement system by transmitting a STOP message to the EIM. As in the start-up sequence, the stop sequence propagates through the EIM, data generator, data processor, and data checker before the stop is complete. Typically, the EC&M computer will make several BER measurements for each test point and average the results, discarding bad sample points, to make a composite BER figure. Then the EC&M computer can set a new signal to noise ratio (E_b/N_o) and/or change other test parameters and execute a new set of BER measurements.

Applications

Since 1985 the DMBERMS has been used in numerous applications at Lewis to characterize the performance of microwave systems and components. These applications include BER performance evaluation of high-power 30- and 20-GHz traveling wave tube amplifiers (ref. 6 and 7), satellite matrix switches (ref. 10), an experimental single channel satellite transponder (ref. 11), a remote microwave link (ref. 12), and a study of the relationship of group delay distortion and BER performance in a satellite communications channel (ref. 13).

In the past, microwave testing and characterization of these components was sufficient to predict their performance in a system environment. With increasing demand for digital satellite communication systems, onboard processing, higher data rates, and more efficient bandwidth utilization, it has become very important to determine the effect that the microwave components will have on modulated digital data. The effect is observable through BER measurements on a digitally modulated data sequence transmitted through actual system hardware.

The DMBERMS was first used to determine the baseline BER performance of its internal modem. Once long-term error-free operation of the digital subsystems of the DMBERMS was verified, the BER contribution of the modulator and demodulator in a back-to-back configuration was easily determined. The resultant baseline BER versus E_b/N_o curve (fig. 12(a)) can then be compared with all other component BER curves, thereby isolating a particular microwave component's contribution to the overall BER performance.

To illustrate the usefulness of the DMBERMS, a short discussion of one of the applications follows. The DMBERMS was used to test two 30-GHz traveling wave tubes in June of 1985. The traveling wave tubes (TWT's) were developed by Hughes Electron Dynamics Division and loaned to the Lewis Advanced Communication Technology Satellite (ACTS) Project Office. The TWT's are similar to the type of amplifier needed for the ACTS. The ACTS will also use SMSK modulation. The project office wished to determine the performance of the ACTS-like TWT's in a digital communication system to enable them to specify a ground terminal amplifier more precisely. Of particular concern were the effects of gain variations in a tube on SMSK modulated digital data.

A frequency conversion system built under contract (NAS3-23966) by LNR Communications, Inc., was used to up convert the modem intermediate frequency of 3.373 GHz to the TWT nominal operating frequency of 30 GHz. As with the modem, the contribution of the frequency conversion system to the BER figure was calibrated out of the TWT BER performance measurement by characterizing the frequency conversion system separately from the TWT's. In this application the Sage microcomputer performed the EC&M functions because mainframe EC&M software was unavailable at the time.

The BER characterization of the two TWT's provided very useful information including future design goals for TWT's and communication systems that use TWT's. The BER testing of

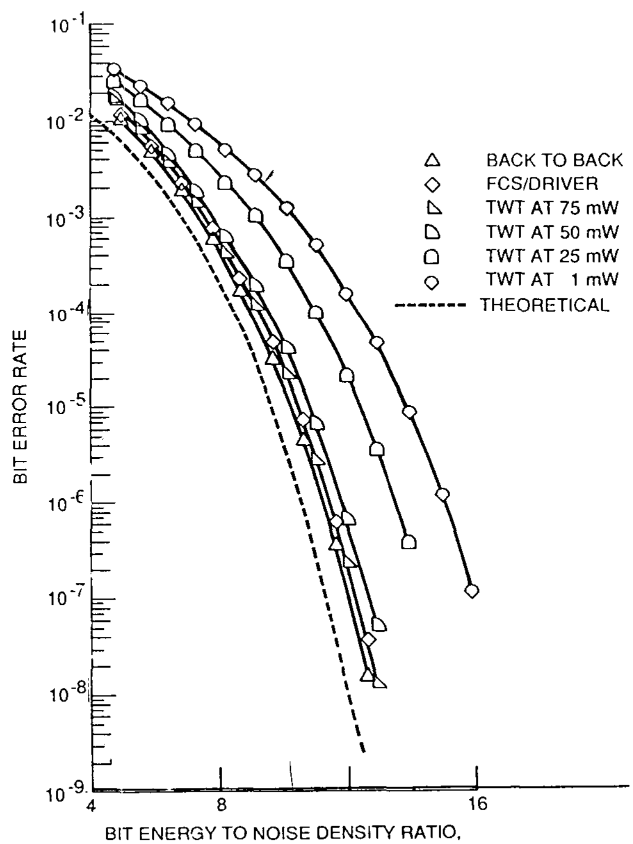


Figure 17.—TWT BER curves.

both tubes established an E_b/N_o requirement of 15.3 dB to achieve a BER performance of 5×10^{-7}, an early ACTS operational requirement (refs. 6 and 7). Microwave testing coupled with the BER testing demonstrated that gain variations did adversely affect the BER performance of the TWT's. Future TWT's can be designed to reduce these gain variations. The BER testing also demonstrated that, contrary to initial assumptions, the tubes performed very well at or near saturation with SMSK modulation. The BER curves of one TWT is shown in figure 17.

Future Plans

The DMBERMS has served as a forerunner for two related efforts: ground terminals for the second phase of the SITE project and a link evaluation terminal for the ACTS. In the second phase of the SITE project, an identical SMSK modem modulates a carrier with bursts of data (instead of a continuous data stream) and operates in both the full-rate (220 Msps) and half-rate (110 Msps) modes. Bit-error-rate measurements can be made at an equivalent data throughput of about 200 Mbps due to the burst overhead and guard times required in TDMA framed operation.

Both the second phase SITE ground terminals and the ACTS link evaluation terminal will use a TDMA controller and compression and expansion FIFO buffer memories to establish and coordinate burst communications and convert serial user data streams to the burst formats compatible with switching and processing satellites. The link evaluation terminal will be used to measure BER through the intermediate frequency matrix switch onboard the ACTS in the early 1990's.

A limitation of the DMBERMS is its use of continuous data at one specific data rate and modulation format. A single-chassis bursted BER measurement system using CRC-16 pseudorandom sequence data is being developed. This system features automatic data acquisition and will allow the user to program the burst duty cycle from 1 to 99 percent and data rates from 1 to over 500 Mbps, and accommodate a variety of modems with a single hardware module change.

Concluding Remarks

A digitally modulated bit-error-rate measurement system (DMBERMS) was developed at NASA Lewis for the System Integration, Test, and Evaluation, (SITE) project. The DMBERMS contains a continuous pseudorandom data source, a bit error rate tester, an SMSK modulator-demodulator, a data processor, a noise generation unit, and a controlling computer. Continuous pseudorandom data at 220 Mbps is formated by the data processor and then modulated. Noise is added to the modulated signal by the noise generation unit. The combined signal and noise is passed through a component or link under evaluation. Then the signal is demodulated, and bit error rate measurements are made. The testing is automated by computer control.

The DMBERMS has been used for a variety of applications in the SITE project, including BER measurements on matrix switches, a remote microwave link, a 20-GHz traveling wave tube, and a laboratory based satellite transponder. The DMBERMS also has many applications outside of the SITE project (e.g., testing of the 30-GHz TWT for the Advanced Communications Technology Satellite Project).

The number of applications can easily be expanded by the use of different modems and frequency conversion systems. Minor modifications can be made to the data processor to control a different modulator-demodulator pair. The BER performance of microwave components could then be measured for different modulation schemes. The present modem also limits the intermediate frequency carrier frequency to 3.373 GHz. Components that are not compatible with this frequency can be tested by using a frequency conversion system to up or down convert the modem carrier frequency for compatibility with the component under test. The data rate can also be adjusted by the data generator to any desired rate up to 220 Mbps.

The digitally modulated BER measurement system provides a unique capability for testing of microwave components of a digital communication system that has not been previously available. The results of the testing are providing very useful data. Not only can the DMBERMS characterize the effects of microwave components on digital data transmission in an overall system, but design goals for microwave components can be determined to achieve a desired BER performance.

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Glossary

ACTS	Advanced Communications Technology Satellite
$\overline{\text{ACK}}$	acknowledge signal
BER	bit error rate
CCITT	Consultative Committee on International Telegraph and Telephone
CPU	central processing unit
$\overline{\text{CTS}}$	clear-to-send signal
$\overline{\text{DAV}}$	data available signal
DMBERMS	digitally modulated BER measurement system
E_b/N_o	signal to noise ratio where E_b is the energy per bit and N_o is the noise power density
ECL	emitter coupled logic
EC&M	experiment, control, and monitor computer
EIM	EC&M interface microcomputer
FIFO	first-in, first-out, as in buffer memories
Mbps	megabits per second
MSK	minimum shift keyed modulation systems
Msps	megasymbols per second
N_{bw}	noise bandwidth of calibration filter
NAK	negative acknowledgement
P_n	noise power
P_s	signal power
PIN	p doped-intrinsic region–n doped diode
QPSK	quadrature phase shift keying
R	the data rate
$\overline{\text{RTS}}$	request-to-send signal
$\overline{\text{RQD}}$	request denied signal
ROM	read only memory
SITE	Systems Integration, Test, and Evaluation project
SMSK	serial minimum shift keying
SS–TDMA	satellite-switched, time division multiple access
SMSK	serial minimum shift keying
START	command initializes the specified generator and creates a transmission request to the ground terminal
STATUS	message
TWT	traveling wave tube
TDMA	time division multiple access
TTL	transistor transistor logic
UWD	unique word detection pulse
VSWR	voltage standing wave ratio
XOR	exclusive or

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15. Supplementary Notes

16. Abstract

The NASA Lewis Research Center has developed a unique capability for evaluation of the microwave components of a digital communication system. This digitally modulated bit-error-rate (BER) measurement system (DMBERMS) features a continuous data digital BER test set, a data processor, a serial minimum shift keying (SMSK) modem, noise generation, and computer automation. Application of the DMBERMS has provided useful information for the evaluation of existing microwave components and of design goals for future components. This paper describes the design and applications of this system for digitally modulated BER measurements.

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